REMARKS

A. Status of Claims

Claims 19-40 are pending in the application prior to this Amendment. Claims 19-40 have been rejected. Claims 19-34, 35, 39, and 40 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,045,610 ("Park et al.") in view of U.S. Patent No. 5,935,320 ("Graef et al.")

Claims 19 and 35 have been amended. Support for the amendment to claim 19 may be found, for example, at Figure 5, at page 18, lines 7-15, and at page 31, lines 12-17 of the Specification. Support for the amendment to claim 35 may be found, for example, at page 34, lines 8-10 and at page 37, lines 27-31 of the Specification.

New claims 41-78 have been added. Support for new claims 41-45, 51-55, and 74-78 may be found, for example, at page 22, lines 5-25 of the Specification. Support for new claims 46, 56, and 73 may be found, for example, at page 34, line 24 through page 35, line 9 of the Specification. Support for new claims 47-50 may be found, for example, at page 27, lines 1-8 of the Specification. Support for new claim 57 may be found, for example, at original claim 19, at page 34, lines 8-10, at page 37, lines 12-17, and at page 37, lines 27-31 of the Specification. Support for new claims 58-72 may be found, for example, at original claims 20-44.

B. Rejection under 35 U.S.C. §103(a)

Reconsideration is requested of the rejection of claims 19-34, 35, 39, and 40 under 35 U.S.C. § 103 (a) being obvious over Park et al. in view of Graef et al.

Claims 19-34

Claim 19, as amended, is directed to a process for preparing a single crystal silicon wafer, the process comprising thermally annealing a single crystal silicon wafer which comprises **thr** concentrically positioned axially symmetric regions. The first

axially symmetric region, which extends radially inward from the circumferential edge, is interstitial dominated (i.e., has silicon self-interstitials as the predominant intrinsic point defect) and is substantially free of agglomerated interstitial defects. The second axially symmetric region, which is located radially inward of the first axially symmetric region, is vacancy dominated (i.e., has vacancies as the predominant intrinsic point defect) and is substantially free of agglomerated vacancy defects. The third axially symmetric region, which is located radially inward of the second axially symmetric region, is vacancy dominated like the second region and comprises agglomerated vacancy defects. The thermal anneal acts to dissolve agglomerated vacancy defects present in the third axially symmetric region within a layer extending from the front side of the wafer towards the central plane.

Park et al. is directed to a method for growing a single crystal ingot such that a wafer sliced from the ingot, as grown, is either "pure" from the axis to the circumferential edge or "semi-pure" such that the ingot has a so-called "vacancy rich" region surrounded by a pure region. According to Park et al. the "pure" region is free of both interstitial agglomerates and vacancy agglomerates whereas the "vacancy rich" region is a region having vacancy agglomerates. That is, Park et al. describe a method for growing an ingot which either has one region (i.e., pure) or two regions (i.e., pure and vacancy rich with defects). In contrast, amended claim 19 requires thermally annealing a wafer having three axially symmetric regions: a first region which is interstitial dominated and free of agglomerated interstitial defects; a second region which is vacancy dominated **and free of agglomerated vacancy defects**; and, a third region which is vacancy dominated and includes vacancy defects. Park et al. nowhere describe or suggest such a wafer. Moreover, Park et al. fail to describe or suggest any region which is both vacancy dominated and substantially free of agglomerated vacancy defects as required by amended claim 19, i.e. the second axially symmetric region. In fact, the only vacancy-type region described by Park et al. is the so-called

"vacancy rich" region which according to Park et al. **does include vacancy agglomerates**.

In addition, Park et al. fails to explicitly disclose annealing wafers cut from their ingot, as admitted by the Office at page 4, first paragraph of the Office action, and certainly fails to disclose or suggest annealing their wafers to dissolve agglomerated vacancy defects. This is not surprising given that Park et al. teaches that the number of vacancy agglomerates may be reduced by controlling the crystal growth process to reduce the radius of the "vacancy rich" region and in fact teaches that the "vacancy rich" region can be completely eliminated to grow a pure crystal. That is, Park et al. teaches away from annealing a wafer grown by their process to dissolve vacancy agglomerates, in that Park et al. teaches that vacancy agglomerates can be avoided during the ingot growth process thereby rendering a post growth thermal treatment, a very costly and time consuming process, unnecessary.

Graef et al. is directed to a process for producing a wafer having a reduced concentration of GOI or COP defects.[1] The process described by Graef et al. requires first growing an ingot **having an increased density of grown in defects**, referred to by Graef et al. as a "defect-rich" single crystal at column 2, lines 56-59. A wafer is then sliced from this "defect-rich" single crystal and subjected to a thermal treatment to dissolve some, **but not all** of the defects. Graef et al. fail to describe or suggest any wafer having the three regions required by claim 19 and certainly fail to suggest any region which is both vacancy dominated and substantially free of agglomerated vacancy defects and as such cannot cure the deficiencies of Park et al. Moreover,

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[1]As noted in the present application and acknowledged by the Office, COP defects are a type of vacancy agglomerate. More precisely, COP defects are agglomerated vacancies or voids which appear on the surface of the wafer as surface defects. Gate oxide integrity or GOI measurement is one method used to determine the presence of these defects. Thus, the presence of GOI and/or COP defects indicates the presence of vacancy agglomerates.

Graef et al. disclose an alternative approach to reducing the concentration of defects wherein a higher concentration of vacancies which are smaller in size must be grown into the crystal during ingot growth so that the thermal anneal of the wafer is more efficient; whereas Park et al. teaches that the concentration of vacancy agglomerates should be minimized during crystal growth and in fact can be completely prevented. Stated differently, Graef et al. teaches away from the process of Park et al.

When considered in their entirety, it is evident that the teachings of Park et al. and Graef et al. not only fail to disclose all of the requirements of claim 19, but in addition are incompatible, hence, the references do not render the Applicants invention obvious under § 103. If the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. MPEP 2143.01; In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). In the instant action, the Graef et al. process requires growing the silicon crystal under conditions which increase the number of vacancy agglomerates prior to subjecting a wafer sliced therefrom to the thermal anneal process taught by Graef et al.; whereas the Park et al. process is intended to reduce and even eliminate the formation of vacancy agglomerates.

Thus, amended claim 19 satisfies the requirements under 35 U.S.C. § 103 (a) over Park et al. in view of Graef et al. because neither reference alone or in combination describes or suggests the requirements of amended claim 19, namely the requirement that the wafer have a first region which is interstitial dominated and free of agglomerated interstitial defect surrounding a second region which is vacancy dominated and substantially free of agglomerated vacancy defects surrounding a third axially symmetric region which is vacancy dominated and has agglomerated vacancy defects. Moreover, as discussed above, Graef et al. teaches a process which is contradictory to the stated intentions of the Park et al.

Claims 20-34 depend directly or indirectly from amended claim 19, and are therefore patentable for the reasons given for amended claim 19.

Claims 35-40

Claim 35, as amended, is directed to a process for preparing a single crystal silicon wafer having a surface layer which is substantially free of agglomerated intrinsic point defects. The process comprises slicing a wafer from a single crystal silicon ingot grown in accordance with the Czochralski method. The wafer comprises a first axially symmetric region extending radially inward from the circumferential edge which is both interstitial dominated and substantially free of agglomerated interstitial defects and a second axially symmetric region, located radially inward of the first axially symmetric region which is vacancy dominated. The wafer is thermally annealed at a temperature in excess of about 1000°C in an atmosphere of hydrogen, argon, oxygen, nitrogen or a mixture thereof to dissolve agglomerated vacancy defects present in the second axially symmetric region within a layer extending inward from the front side of the wafer **such that the layer is substantially free of agglomerated intrinsic point defects.**

The Office recognizes that Park et al. fail to disclose annealing wafers. Indeed, one skilled in the art would have no reason to anneal the preferred embodiment of Park et al., which is purportedly an agglomerate free wafer. That is, as discussed above with regards to amended claim 19, Park et al. teaches that agglomerated defects may be avoided in the crystal growth process rendering the addition of a costly thermal annealing step unnecessary.

Graef et al. fail to disclose or suggest an anneal process which forms a surface layer in a wafer **which is substantially free of agglomerated intrinsic point defects.** To the contrary, Graef et al. disclose that " the larger defects **are not removed** during the annealing. The larger defects remain," at column 3, lines 1-13 (emphasis added). Indeed, according to Examples 1-3 and the associated figures, Graef et al. detect defects in every wafer which has been subjected to an annealing process. Significantly,

the defects detected by Graef et al. are COP type defects which, as discussed above, are vacancy agglomerates that intersect the surface of the wafer. In contrast, claim 35 requires the formation of a surface layer that is substantially free of agglomerated intrinsic point defects.[2] Accordingly, Graef et al. fail to cure the defect of Park et al.

Thus, amended claim 35 satisfies the requirements under 35 U.S.C. § 103 (a) over Park et al. in view of Graef et al. because neither reference alone or in combination describes or suggests the requirements of amended claim 35, namely the wafer is thermally annealed such that the surface layer is substantially free of agglomerated intrinsic point defects.

Claims 35-40 depend directly or indirectly from amended claim 35, and are therefore patentable for the reasons given for amended claim 35.

C. New Claims 41-78

New Claims 41-56

New claims 41-50 and 51-56 depend from amended claims 19 and 35 respectively and therefore are patentable for the reasons given above with regard to amended claims 19 and 35. New claims 41and 51 are further directed to the cooling of the ingot from which the wafer of amended claims 19 and 35 is sliced, wherein the ingot is cooled at a rate which ranges from about 0.1 to about 3.0 °C/min. New claims 42 and 52 further describe cooling the ingot from about 0.1 to about 3.0 °C/min through a temperature range from solidification to about 800°C. Park et al. fails to disclose or suggest a cooling rate for an ingot through any defined temperature ranges. Graef et al. require that the wafers to be annealed are obtained from an ingot which has been

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[2] According to the Specification of the present invention at page 37, lines 27-31, "substantially free of agglomerated defects" means a concentration of agglomerated defects which is less than the detection limit of these defects. Graef et al. detected defects.

cooled such that the ingot is held within a temperature range between 850°C and 1100°C for less than 80 minutes, which corresponds to a cooling rate of **3.125** °C/min. By requiring a cooling rate in excess of the rates described in new claims 41 and 51, Graef teaches away from the present invention, especially with regard to the temperature ranges described in new claims 42 and 52, which explicitly bound the temperature range at which Graef et al. disclose the elevated cooling rate. Thus, new claims 41, 42, 51, and 52 are separately patentable over Park et al. in view of Graef et al. New claims 43-45 depend from new claim 42 and new claims 53-55 depend from new claim 52 and are further patentable for the reasons given above for new claims 42 and 52.

New Claims 57-78

New claim 57 is directed to a process for preparing a single crystal silicon wafer having a surface layer which is substantially free of agglomerated intrinsic point defects. The wafer is sliced from a single crystal silicon ingot grown in accordance with the Czochralski method, and the wafer comprises a first axially symmetric region extending radially inward from the circumferential edge in which silicon self-interstitials are the predominant intrinsic point defect and which is substantially free of agglomerated interstitial defects and a second axially symmetric region, located radially inward of the first axially symmetric region, in which vacancies are the predominant intrinsic point defect. The process comprises thermally annealing the wafer at a temperature in excess of about 1000°C in an atmosphere of hydrogen, argon, oxygen, nitrogen or a mixture thereof to dissolve agglomerated vacancy defects present in the second axially symmetric region within a layer extending inward from the front side of the wafer **such that the layer is substantially free of agglomerated intrinsic point defects**. New claim 57 is similar to amended claim 35 in that the thermal anneal acts to dissolve agglomerated vacancy defects such that a surface layer of the wafer is substantially free from agglomerated vacancy defects. New claim 57 is therefore patentable over the

cited references for the reasons given above for amended claim 35. New claims 58-73 depend directly or indirectly from new claim 57 and are therefore patentable for the reasons given for new claim 57. Additionally, new claims 74-78 are further patentable for the reasons given above for new claims 41-45 and 51-55.

D. Supplemental Information Disclosure Statement

The Information Disclosure Statement filed in the present application on May 16, 2002 stated, "Applicants are not submitting copies of Reference Nos. 1-40, 42, 45-61, 64-68, 70-91, 93-110, 112-126, 128-136 and 139-140, which were previously made of record in application Serial No. 09/385,108." However, the identified application was incorrect. The correct reference is to application Serial No. **09/416,998**, which was identified elsewhere in the IDS as the parent of the present divisional application. Applicants enclose a Supplemental Information Disclosure Statement to remedy the defect in the IDS originally filed in the present application.

CONCLUSION

In view of the foregoing, Applicants respectfully submit that claims 19-40 as amended and that new claims 41-78, which are now pending in this application, satisfy the requirements for patentability. Favorable reconsideration and allowance of these claims are therefore respectfully requested.

Applicants enclose a check for $1,794.00 to cover the fee for a three-month extension of time, the extra claims fee, and the fee for a Supplemental IDS. The Examiner is authorized to charge any underpayment or to credit any overpayment of the above referenced fees to Deposit Account No. 19-1345.

Respectfully submitted,

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